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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, CAMVAN T	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,520	MUKHERJEE, SHUBHENDU S.	
	Examiner	Art Unit	
	CamVan T. Nguyen	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/02/04, 11/14/05 & 12/22/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *9-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/8/04, 11/14/05,* 12/22/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-8, drawn to transferring data from computer to computer, classified in class 709, subclass 236.

   II. Claims 9-11, drawn to transferring data via a shared memory, classified in class 709, subclass 213.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination II has separate utility such as combining a plurality of entries in a merge buffer that are destined to the same processor into a single network packet. See MPEP § 806.05(d).

3. Because these inventions are independent or distinct for the reasons given above and have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

4. Because these inventions are independent or distinct for the reasons given above and the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Michael Nesheiwat on May 17, 2006 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-8. Affirmation of this election must be made by applicant in replying to this Office action. Claims 9-11 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: figure 1, reference characters 1-4 and figure 2, reference characters 1-4. The drawings are further objected to because:

a. Figure 1, step 2 recites the limitation "and/or" which is not consistent with the specification. The specification discloses combining read miss requests that are headed to the same processor "*and*" that occur in bursts (p5, lines 12-13).

b. Figure 4 contains the following elements that are neither described nor referred to by the specification: IO, CS, 1/2W, and CSI.

7. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being

amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. Claims 1 & 4 recite the limitation "to that same processor". There is insufficient antecedent basis for this limitation in the specification. The specification teaches forwarding the single network packet "into the network" (p5, lines 22-23). For purposes of examination, "to that same

processor" is construed to be "into the network". Furthermore, claims 1 & 4 recite the limitation "the MAF controller". There is insufficient antecedent basis for this limitation in the claim.

b. Claims 2 & 5 recite the limitation "a program stream through an array in a scientific application". This is indefinite. It is unclear what constitutes "a program stream through an array" as well as what constitutes a "scientific" application.

c. Claim 7 recites the limitation "to be transmitted in the network". There is insufficient antecedent basis for this limitation in the specification. The specification teaches " transmits it into the network" (p6, line19). For purposes of examination "in the network" is construed as "into the network".

d. Claims 3, 6 & 8 are being rejected as incorporating the deficiencies of a claim upon which it depends.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, and further in view of the Shibayama et al. reference "An

Optical Bus Computer Cluster with A Deferred Cache Coherence Protocol" and well known practices in the art.

a. For claims 1 & 4, the applicant's admitted prior art teaches generating an entry in a Miss Address File (MAF) for each of the plurality of read miss requests (page 4 line 27 – page 5 line 6). The applicant's admitted prior art does not teach delaying the MAF controller from forwarding the plurality of read miss requests for a predetermined number of cycles; combining the plurality of read miss requests that are destined to the same processor into a single network packet; and forwarding the single network packet to that same processor; nor does it teach the additional limitation of claim 4 that the plurality of read miss requests occur in bursts. The Shibayama et al. reference teaches a method for combining a plurality of requests into a single network packet for a network of a plurality of processors (Abstract, lines 4-7, "Optical Bus Computer Cluster") comprising delaying forwarding the plurality of requests for a predetermined number of cycles (Abstract, 2nd paragraph, lines 6-8; page 177, section 4, 1st paragraph, lines 1-4, "synchronization point"; figure 2(b)); and combining the plurality of requests (page 178, right hand column, last paragraph, line 2, "several coherence transactions") that are destined to the same processor (page 178, right hand column, last paragraph, "sub-blocks in the same cache line" belongs to one processor) into a single network packet (page 178, right hand column, last paragraph,

"combined into one coherence transaction"); and forwarding the single network packet to that same processor (*into the network*) (implied). It teaches that this method is particularly useful for effectively reducing the amount of coherence transactions on the network (Abstract, 2nd paragraph, line12 – 3rd paragraph, line 3) thereby improving overall system performance (page 176, left hand column, 3rd paragraph, lines 4-6). The prior art discusses combining a plurality of invalidation requests in particular and does not specifically teach combining a plurality of read miss requests. However, since read miss requests are also a type of coherence transaction that causes network traffic, it would have been obvious to a person having ordinary skill in the art at the time of invention to implement the deferred coherence transaction taught by the Shibayama et al. reference with the system taught by the applicant's admitted prior art to combine the read miss requests in order to improve overall system performance by reducing the amount of coherence transactions on the network. Delaying the MAF controller naturally follows to allow for the plurality of read miss requests to be consolidated into a single network packet. Burst mode accesses are well known in the art. It is further well known that in a burst mode transaction, a single address is dispatched and data from multiple consecutive address locations is expected in return. Because the addresses are consecutive, a miss in any one of those locations will result in a read miss to all the locations. Official notice

is taken. Therefore, read miss requests will occur in bursts whenever there is a cache read miss to a request in burst mode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined these read miss requests that occur in bursts into a single network packet to effectively reduce the amount of coherence transactions on the network thereby improving overall system performance as discussed above.

b. For claims 2 & 5, it is well known to use burst mode accesses in scientific applications and database programs. Official notice is taken. Furthermore, it would have been obvious to a person having ordinary skill in the art at the time of the invention that it is advantageous to implement this network traffic reduction scheme to improve overall system performance regardless of any type of program that is being run, including a scientific application or a database program.

c. For claims 3 & 6, the Shibayama et al. reference teaches the network is a cache-coherent shared memory configuration (Abstract, 1st paragraph, lines 4-7, "cache-coherent non-uniform memory access"; page 177, section 3, 1st paragraph, lines 1-3).

d. For claim 7, the applicant's admitted prior art teaches identifying a plurality of exclusive access requests by at least one of the plurality of processors for writing a cache block to a local cache (page 6, lines 8-10). It teaches that when a processor needs to write a block to a local cache, the

processor must first request exclusive access to write this block (page 6, lines 8-10). It does not teach combining the plurality of exclusive access requests into a single network packet to be transmitted in the network. The Shibayama et al. reference teaches a method for combining a plurality of requests into a single network packet for a network of a plurality of processors (Abstract, lines 4-7, "Optical Bus Computer Cluster") comprising: identifying a plurality of requests by at least one of the plurality of processors for writing a cache block to a local cache (page 178, left hand column, 1st paragraph, lines 1-3 & 8-11, "writes to ... cache lines"); and combining the plurality of requests into a single network packet to be transmitted in the network (page 178, right hand column, last paragraph). It does not teach that the requests are exclusive access requests. It teaches invalidation requests. However, a person having ordinary skill in the art at the time of the invention would have recognized the need to send invalidations (i.e. request "exclusive" access as is taught by the applicant's admitted prior art on page 6, lines 8-11) to other nodes holding copies of a cache block in order to obtain exclusive access to a block for writing. Thus, it would have been obvious to implement the method taught by the Shibayama reference with the exclusive access requests discussed by the applicant's admitted prior art in order to reduce the amount of coherence transactions on the network thereby improving system performance.

e. For claim 8, the method of claim 7 wherein the plurality of exclusive access requests is granted by a home node in the network is also taught by applicant's admitted prior art (page 5 line 26 – page 6 line 12, "Typically...").

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Rothschild et al. (U.S. Patent No. 5,822,523) teaches aggregating messages received during a specified time period and then sending an aggregated message to the targeted hosts to reduce message traffic between hosts in a networked interactive application.

b. Blackmore et al. (U.S. Patent No. 6,389,478) teaches a method of grouping two or more I/O vectors into a single packet to be transferred across a distributed computing environment comprising a plurality of processing nodes coupled together over a network.

c. Bogin et al. (U.S. Patent Pub. No. 2002/0087801 A1) teaches combining two or more consecutive write requests to cache.

Examiner Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CamVan T. Nguyen whose telephone number is 571-

270-1039. The examiner can normally be reached on Monday -Thursday 7:30am - 5:00pm and alternate Friday 7:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Robertson can be reached on 571-272-4186. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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06/14/2006

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